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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,966	01/28/2004	Shou-Tsung Wang	MTKP0034USA	1965

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EXAMINER	
NGUYEN, TUAN HOANG	
ART UNIT	**PAPER NUMBER**
2618	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/11/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/11/2007.

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Office Action Summary	Application No.	Applicant(s)	
	10/707,966	WANG ET AL.	
	Examiner	Art Unit	
	Tuan H. Nguyen	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,and 7-11* is/are rejected.

7)☒ Claim(s) *4 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response To Arguments

1. Applicant's arguments, see applicant's remarks, filed on 01/18/2007, with respect to the rejection(s) of claims 1-11 under 35 U.S.C § 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Gu (US PUB. 2003/0072393) and Greer (U.S PAT. 6,545,569).

Claim Rejections - 35 USC § 112

2. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation " at least **second** calibration device " in page 3 line 18. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5, and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu (US PUB. 2003/0072393) in view of Greer (U.S PAT. 6,545,569).

Consider claim 1, Gu teaches an analog demodulator used in a low-IF receiver, the analog demodulator (110) comprising: a receiving circuit (108) for receiving in-phase IF (intermediate frequency) signals and quadrature-phase IF signals (fig. 1A page 2 [0032]); a reference source for providing a reference clock (fig. 2 page 3 [0040]); a local oscillator signal generator electrically connected to the reference source for transferring the frequency of the reference clock to a predetermined frequency (fig. 1A page 2 [0032] and fig. 2 page 3 [0040] i.e., the local oscillator (114) generated reference clock to a predetermined frequency and input to mixers (120, 130)).

Gu does not explicitly show that at least one first calibration device connected to the receiving circuit for reducing DC components of the in-phase IF signals and the quadrature-phase IF signals; and at least one mixer electrically connected to the local oscillator signal generator and the at least one first calibration device for processing the pair of quadrature signals; wherein the at least one first calibration device is serially connected between the receiving circuit and the at least one mixer and comprises a filter for reducing DC components of the in phase IF signals and the quadrature-phase IF signals.

In the same field of endeavor, Greer teaches at least one first calibration device connected to the receiving circuit for reducing DC components of the in-phase IF signals and the quadrature-phase IF signals (fig. 1 col. 4 lines 15-28); and at least one mixer (MX) electrically connected to the local oscillator signal generator (VCO) and the at least one first calibration device (FD) for processing the pair of quadrature signals (fig. 1 col. 4 lines 1-14); wherein the at least one first calibration device is serially connected between the receiving circuit (DEM) and the at least one mixer (MX) and comprises a filter for reducing DC components of the in phase IF signals and the quadrature-phase IF signals (fig. 1 col. 4 lines 1-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, at least one first calibration device connected to the receiving circuit for reducing DC components of the in-phase IF signals and the quadrature-phase IF signals; and at least one mixer electrically connected to the local oscillator signal generator and the at least one first calibration device for processing the

pair of quadrature signals; wherein the at least one first calibration device is serially connected between the receiving circuit and the at least one mixer and comprises a filter for reducing DC components of the in phase IF signals and the quadrature-phase IF signals, as taught by Greer, in order to provide the filters are particularly well-suited for incorporation in integrated circuits by virtue of reducing the physical size of the required capacitors and reduction of time-dependent inertia and filtering device intended to eliminate a DC component from an electronic signal.

Consider claims 2 and 8, Greer further teaches the filter is a notch filter or a high pass filter (col. 1 lines 40-49).

Consider claim 3, Greer further teaches at least one second calibration device electrically connected to the corresponding mixer for reducing DC offset generated by the mixer (col. 4 lines 15-28).

Consider claim 5, Gu teaches an analog demodulator used in a low-IF receiver, the analog demodulator comprising: a receiving circuit for receiving a pair of quadrature signals (fig. 1A page 2 [0032]); a reference source for providing a reference clock (fig. 2 page 3 [0040]); a local oscillator signal generator electrically connected to the reference source for lowering the frequency of the reference clock to a predetermined frequency

(fig. 1A page 2 [0032] and fig. 2 page 3 [0040] i.e., the local oscillator (114) generated reference clock to a predetermined frequency and input to mixers (120, 130)); at least one mixer electrically connected to the local oscillator signal generator (fig. 1A page 2 [0032]) and the receiving circuit for respectively processing the pair of quadrature signals (fig. 1A page 2 [0032]).

Gu does not explicitly show that at least one second calibration device electrically connected to the corresponding mixer for erasing DC offset generated by the mixer.

In the same field of endeavor, Greer teaches at least one second calibration device electrically connected to the corresponding mixer for erasing DC offset generated by the mixer (col. 1 lines 40-49).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, at least one second calibration device electrically connected to the corresponding mixer for erasing DC offset generated by the mixer, as taught by Greer, in order to provide the filters are particularly well-suited for incorporation in integrated circuits by virtue of reducing the physical size of the required capacitors and reduction of time-dependent inertia and filtering device intended to eliminate a DC component from an electronic signal.

Consider claim 7, Greer further teaches at least one first calibration device connected to the receiving circuit for reducing DC components of the pair of quadrature signals (fig. 1 col. 4 lines 1-14); wherein the at least one first calibration device is serially

connected between the receiving circuit (DEM) and the at least one mixer (MX) and comprises a filter for reducing DC components of the pair of quadrature signals (fig. 1 col. 4 lines 1-28).

5. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu in view of Greer and further in view of Wu et al. (U.S PAT. 6,545,569 hereinafter, "Wu").

Consider claim 9, Gu teaches an analog demodulator used in a low-IF receiver, the analog demodulator being an image-rejected analog demodulator with image-rejection capability, the analog demodulator comprising: a receiving circuit for receiving a pair of quadrature IF (intermediate frequency) signals (page 2 [0032] and [0033]); a reference source for providing a reference clock (fig. 2 page 3 [0040]); a local oscillator signal generator electrically connected to the reference source for transferring the frequency of the reference clock to a predetermined frequency (fig. 1A page 2 [0032] and fig. 2 page 3 [0040] i.e., the local oscillator (114) generated reference clock to a predetermined frequency and input to mixers (120, 130)).

Gu does not explicitly show that at least one mixer electrically connected to the local oscillator signal generator and a calibration device for processing the pair of quadrature signals; and the calibration device is serially connected between the receiving circuit (DEM) and the at least one mixer (MX) and comprises a filter for reducing DC components of the pair of quadrature signals.

In the same field of endeavor, Greer teaches at least one mixer electrically connected to the local oscillator signal generator and a calibration device for processing the pair of quadrature signals (fig. 1 col. 4 lines 1-28); and the calibration device is serially connected between the receiving circuit (DEM) and the at least one mixer (MX) and comprises a filter for reducing DC components of the pair of quadrature signals (fig. 1 col. 4 lines 1-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, at least one mixer electrically connected to the local oscillator signal generator and a calibration device for processing the pair of quadrature signals; and the calibration device is serially connected between the receiving circuit (DEM) and the at least one mixer (MX) and comprises a filter for reducing DC components of the pair of quadrature signals, as taught by Greer, in order to provide the filters are particularly well-suited for incorporation in integrated circuits by virtue of reducing the physical size of the required capacitors and reduction of time-dependent inertia and filtering device intended to eliminate a DC component from an electronic signal.

Gu and Greer, in combination, fails to teaches at least one mixer electrically connected to the local oscillator signal generator and a calibration device for processing the pair of quadrature signals.

However, Wu teaches a filtering device (32) electrically connected to the local oscillator signal generator (38) for reducing high-order harmonic components generated by the local oscillator signal generator (fig. 2 col. 8 lines 53-64).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Wu into view of Gu and Greer, in order to provide full integration of the transceiver onto a single IC for a low cost, low power, reliable and more compact solution.

Consider claim 10, Gu further teaches the image-rejection ability of the analog demodulator relies on whether the quadrature phase difference among four input signals of the local oscillator signal generator is 90 degrees and whether amplitudes of the four input signals of the local oscillator signal generator are the same (page 3 [0033]).

Consider claim 11, Gu further teaches the filtering device is a poly-phase filter, a low pass filter, or a digital filter (page 4 [0052]).

Allowable Subject Matter

6. Claims 4 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any response to this action should be mailed to:

Mail Stop_____ (Explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Facsimile responses should be faxed to:

(571) 273-8300

Hand-delivered responses should be brought to:

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401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is (571) 272-8329. The examiner can normally be reached on 8:00Am - 5:00Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Maung Nay A. can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information Consider the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Nguyen
Examiner
Art Unit 2618 T. N

NAY MAUNG
SUPERVISORY PATENT EXAMINER